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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,464	11/24/2003	Anthony Correale JR.	YOR920030358US1	4074

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EXAMINER	
LEVIN, NAUM B	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/720,464	CORREALE ET AL.	
	Examiner	Art Unit	
	Naum B. Levin	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10-31* is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/24/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: the cross-reference information must be updated and the attorney docket numbers must deleted throughout the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-2 and 4-9 are rejected under 35 U.S.C. 102(e) as being unpatentable by Bansal (US Patent 6,944,843).

2. As to claim 1 Bansal discloses:

An integrated circuit (IC) comprising:

a plurality of circuit rows, at least one row of said plurality of circuit rows including three or more voltage islands (The core area of a cell-based ASIC chip includes rows ... of core cells ... circuits for each logic function are placed using a block of core cells. ... One logic block area can be different than another logic block area. All

circuits within a logic block use only one of the power supply voltages – col.2, ll.53-55; col.2, ll.65-67; col.3, ll.1-7);

at least one low voltage island in said at least one row, circuit elements in each said at least one low voltage island being powered by a low voltage (Vddl) supply (logic blocks operating at a relatively lower clock frequency are synthesized using a circuit macro library designed for lower power supply voltages - col.2, ll.58-61); and

at least one high voltage island in said at least one row, circuit elements in each said at least one high voltage island being powered by a high voltage (Vddh) supply, Vddh being a higher voltage than Vddl (The logic blocks operating at a relatively higher clock frequency are synthesized using a circuit macro library designed for higher power supply voltages - col.2, ll.55-58).

3. As to claims 2 and 4-9 Bansal recites:

(2) An IC as in claim 1 wherein said at least one low voltage island is a low voltage macro (col.2, ll.58-61);

(4) An IC as in claim 1 wherein said at least one low voltage island is a low voltage cell (col.2, ll.58-61; col.2, ll.65-67; col.4, ll.15-30);

(5) An IC as in claim 1 wherein said at least one low voltage island spans two or more of said plurality of circuit rows (col.2, ll.65-67; col.3, ll.1-7);

(6) An IC as in claim 5 wherein said at least one low voltage island is surrounded by a plurality of high voltage islands (col.5, ll.59-67; col.6, ll.1-6; Fig.6);

(7) An IC as in claim 6 wherein said plurality of high voltage island include a high voltage standard cell, a high voltage latch and a high voltage macro (col.2, ll.55-58; col.4, ll.15-30);

(8) An IC as in claim 1 wherein said at least one high voltage island includes at least one level converter receiving an output from said at least one low voltage island (col.4, ll.31-33);

(9) An IC as in claim 8 wherein said at least one low voltage island comprises a plurality of low voltage islands and said at least one level converter comprises a plurality of level converters (col.3, ll.45-49).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable by Bansal in view of Lichtensteiger (US Patent 6,990,645).

With respect to claim 3 Bansal teaches the features above but lacks an integrated circuit, wherein at least one low voltage island is a low voltage latch.

5. As to claim 3 Lichtensteiger in view of Bansal teaches:

(3) An IC as in claim 1 wherein said at least one low voltage (minimum operating voltage of voltage island) island is a low voltage latch (col.3, ll.17-34; col.9, ll.24-32);

It would have been obvious to a person of ordinary skills in the art at the time the invention was made to employ Lichtensteiger's teaching regarding the integrated circuit, wherein at least one low voltage island is a low voltage latch and use it in Bansal's invention to increase an efficiency of the integrated circuit design by improving a static timing analysis based on minimum operating voltage of voltage island, wherein island is a low voltage latch.

Allowable Subject Matter

6. Claims 10-31 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or suggest or render obvious:

A method/program of reducing power in an integrated circuit design, said method comprising the steps of: placing and wiring circuit elements for timing closure at a first supply voltage; assigning a plurality of circuit elements for replacement as low voltage circuit elements in a logic aware supply voltage assignment, wherein said low voltage circuit elements operate at a supply voltage below said first supply voltage; optimizing level converter placement; and adjusting assignment of low voltage circuit elements responsive to cell placement in a physically aware voltage re-assignment.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Naum B. Levin whose telephone number is 571-272-1898. The examiner can normally be reached on M-F (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

STACY A. WHITMORE
PRIMARY EXAMINER

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